

FIG. 1

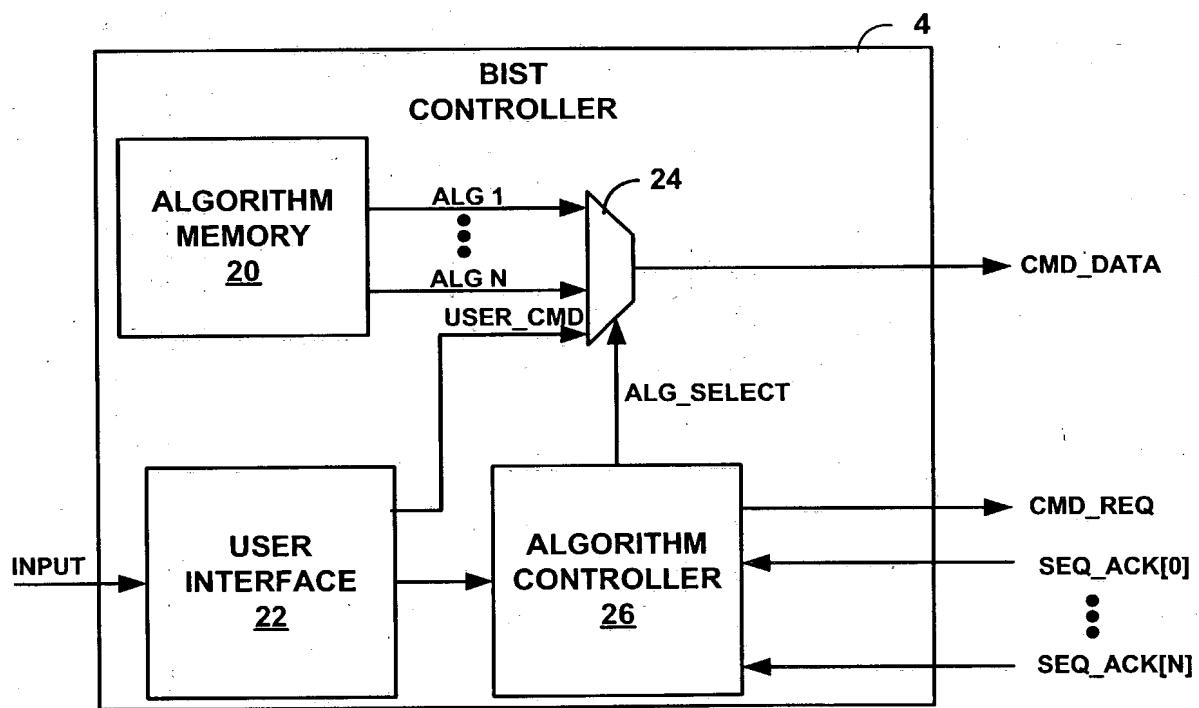


FIG. 2

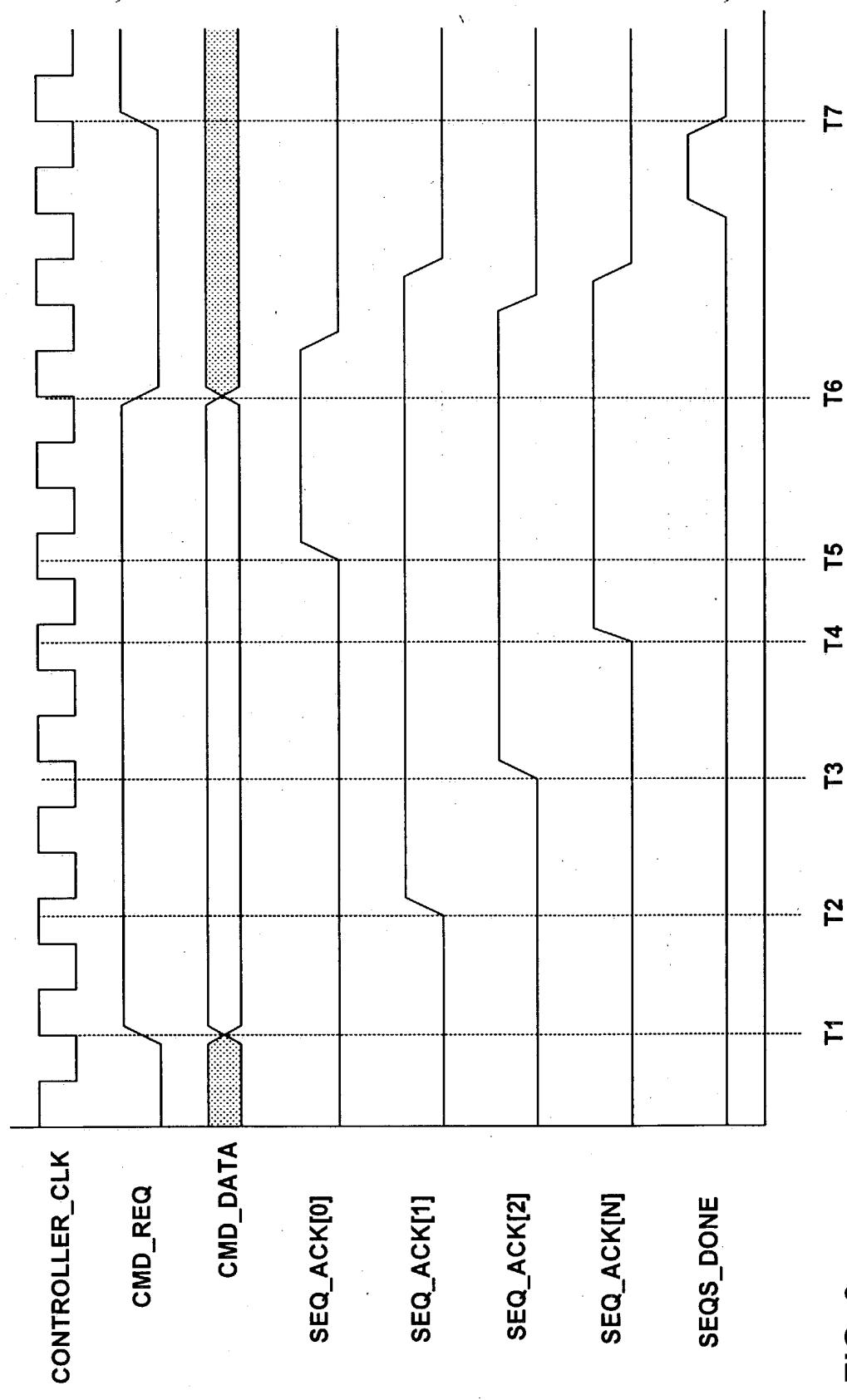


FIG. 3

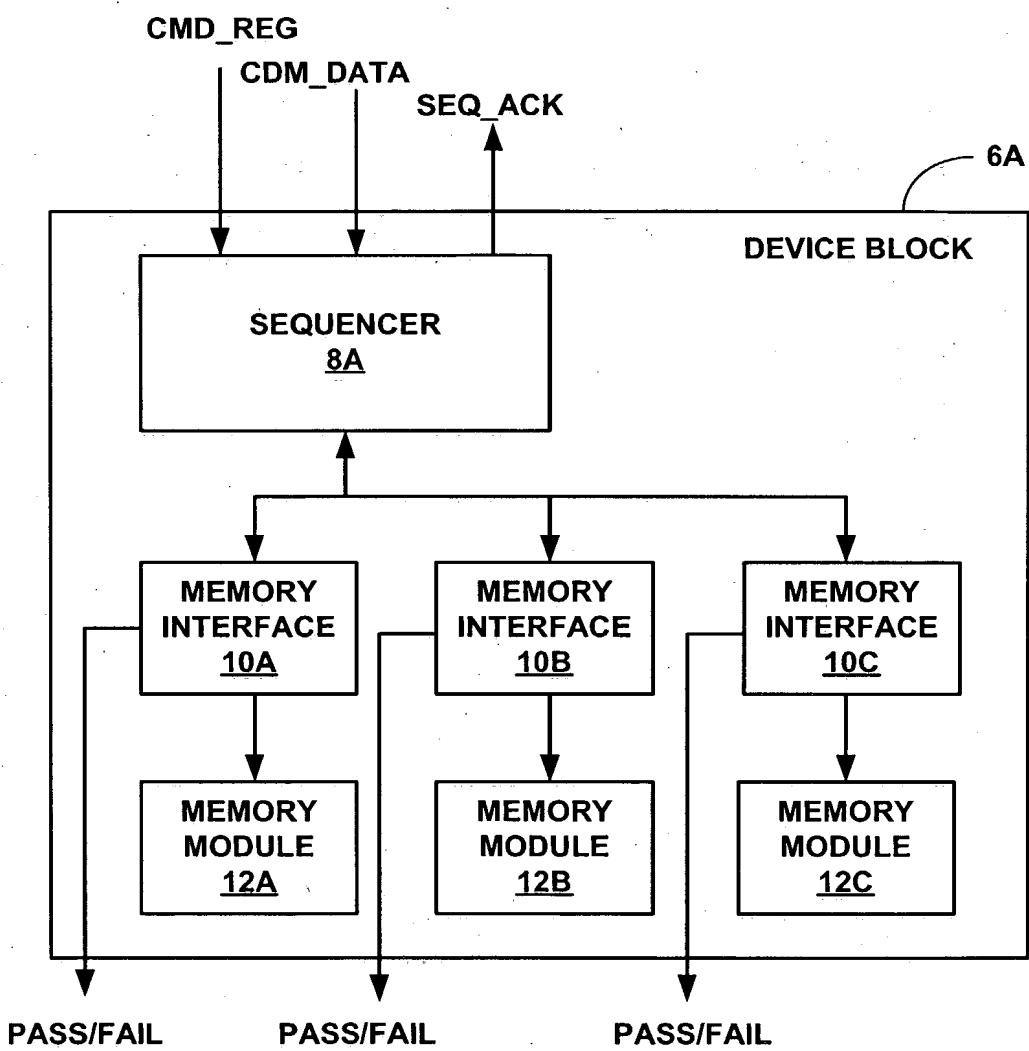


FIG. 4

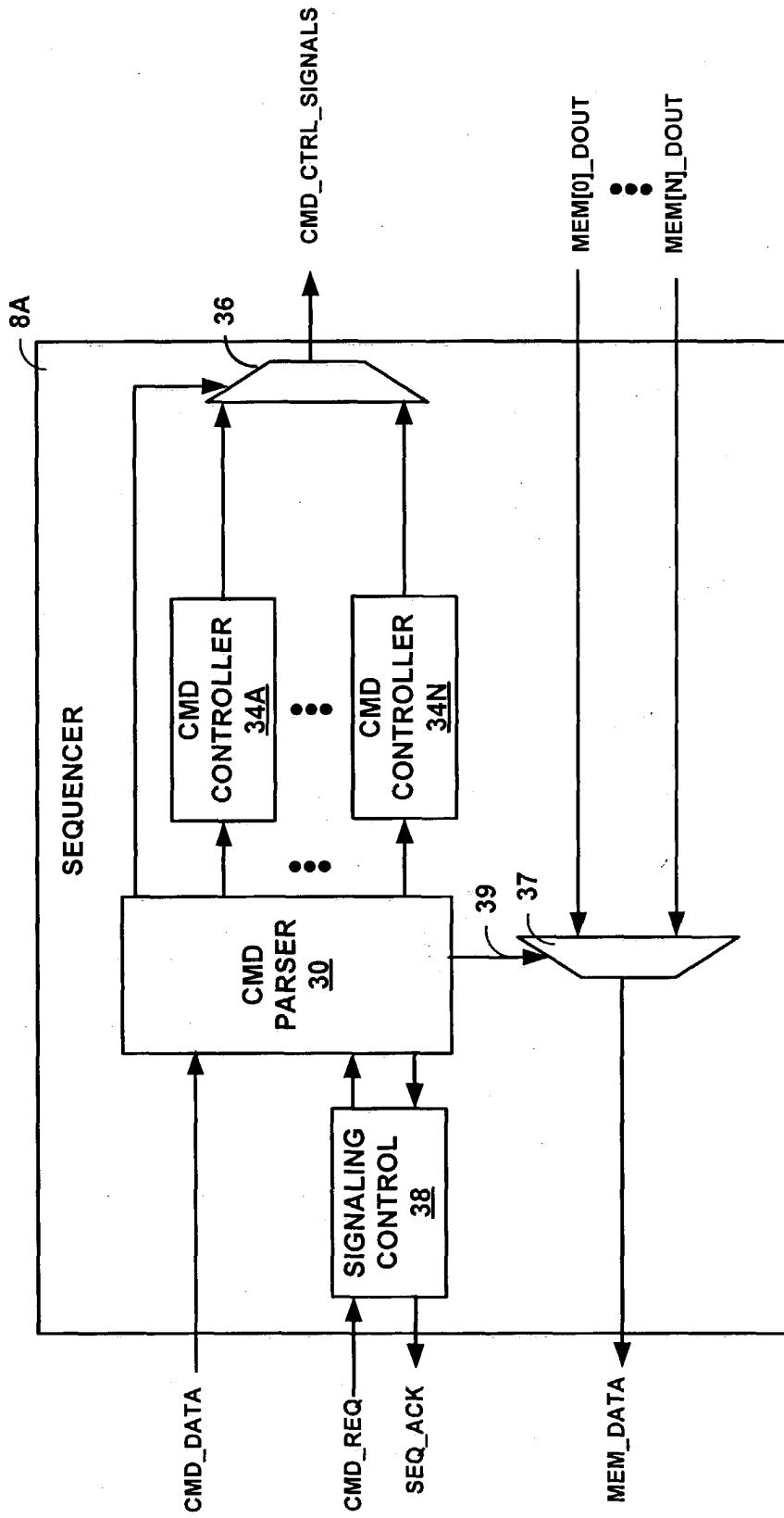


FIG. 5

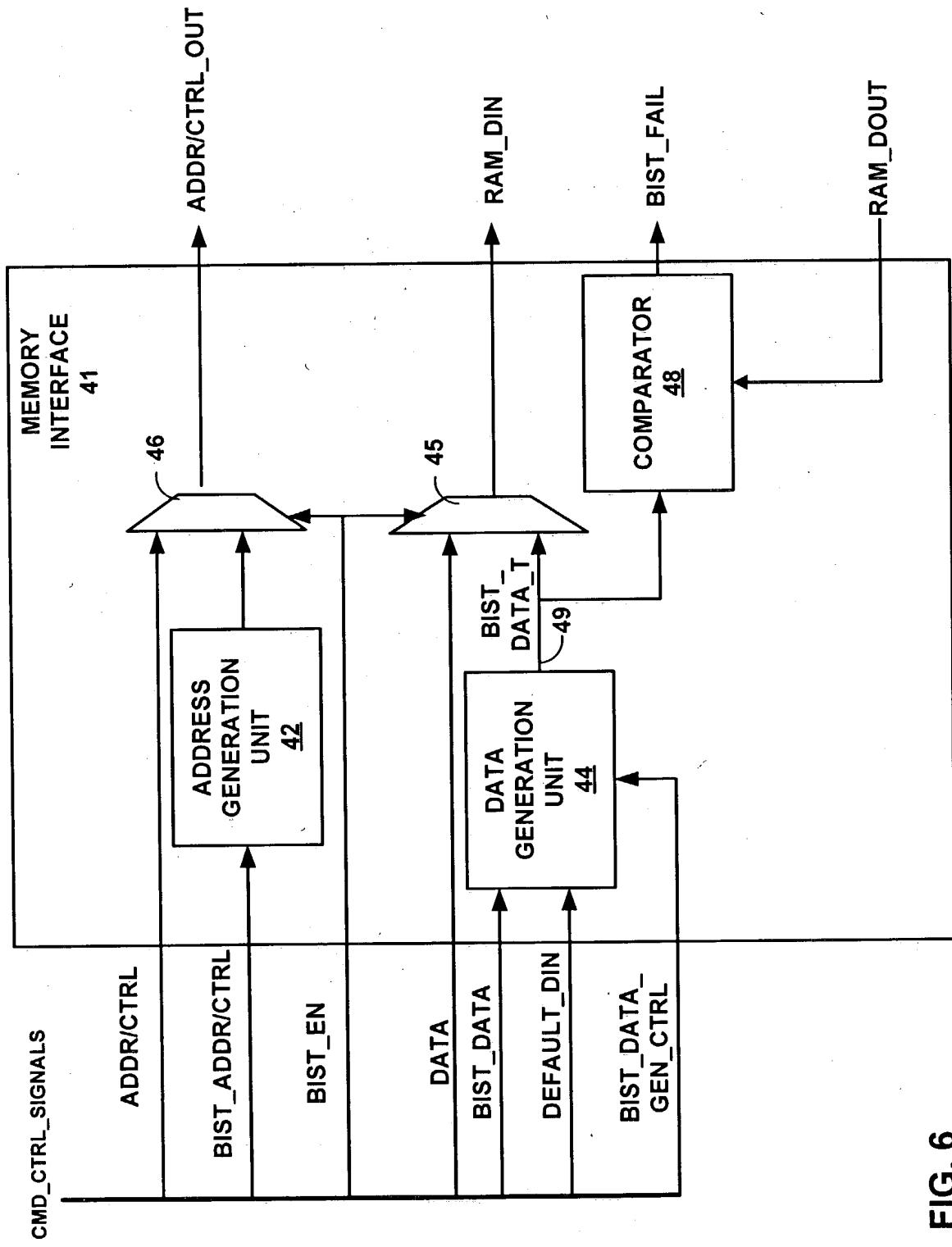


FIG. 6

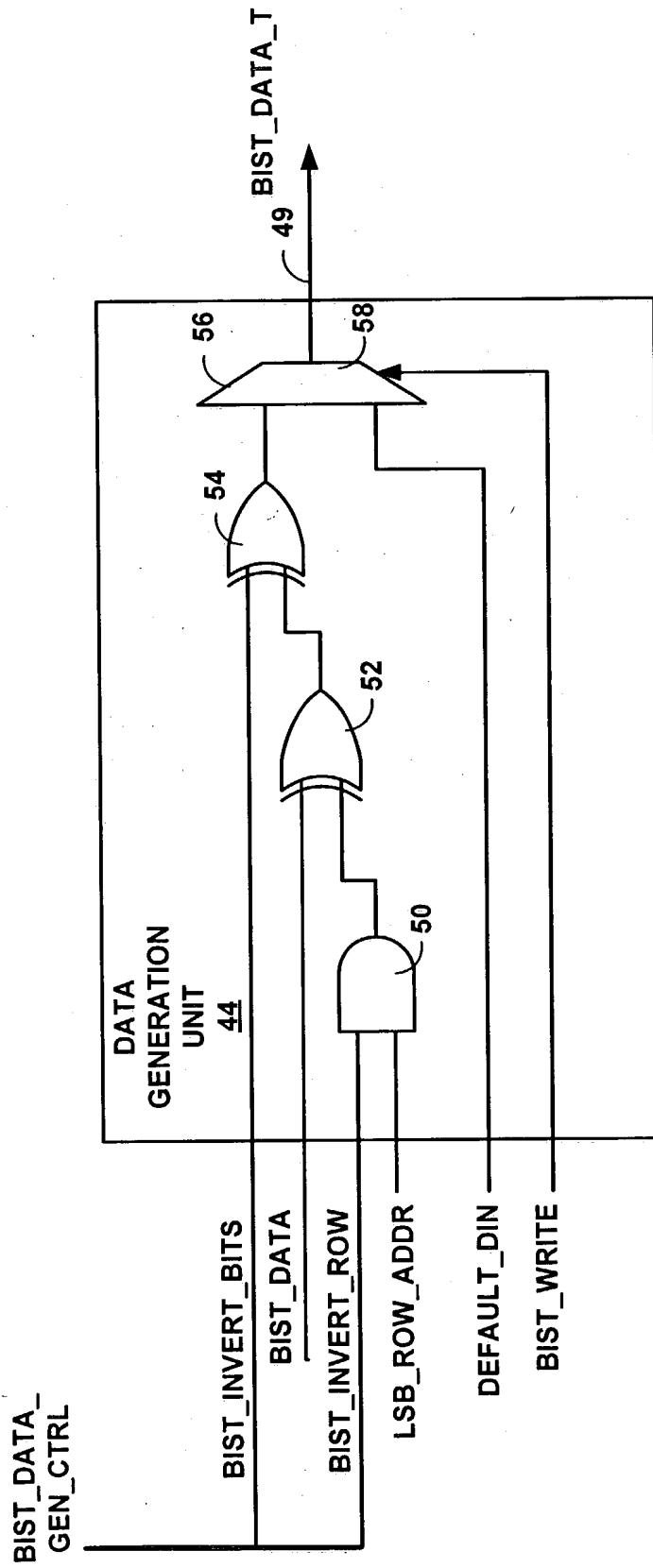


FIG. 7

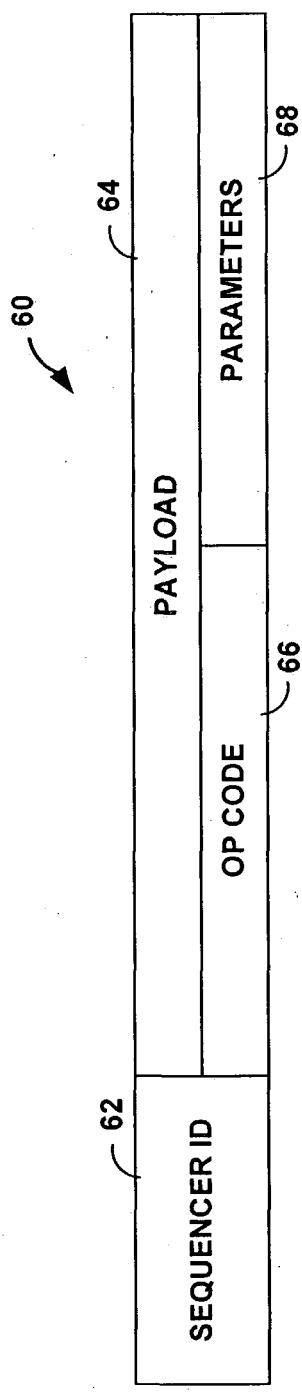


FIG. 8

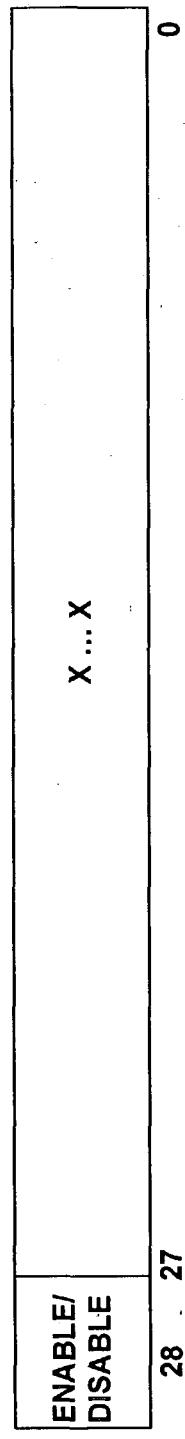


FIG. 9A

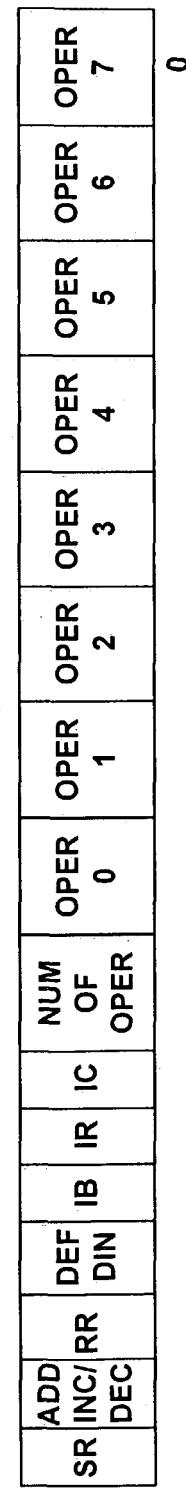


FIG. 9B

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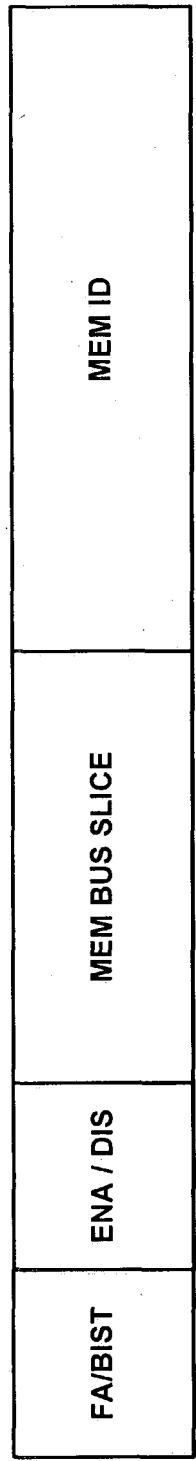


FIG. 9C

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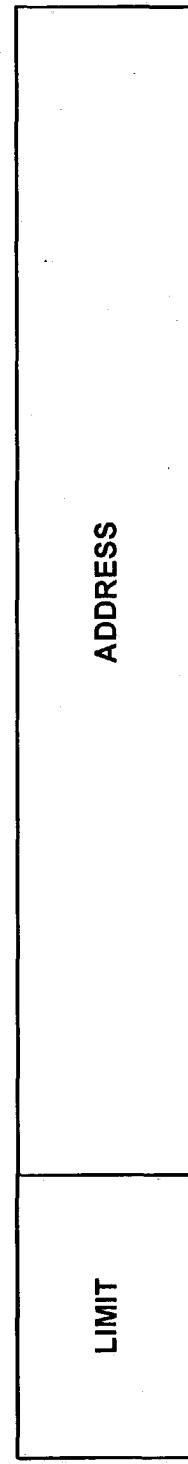


FIG. 9D

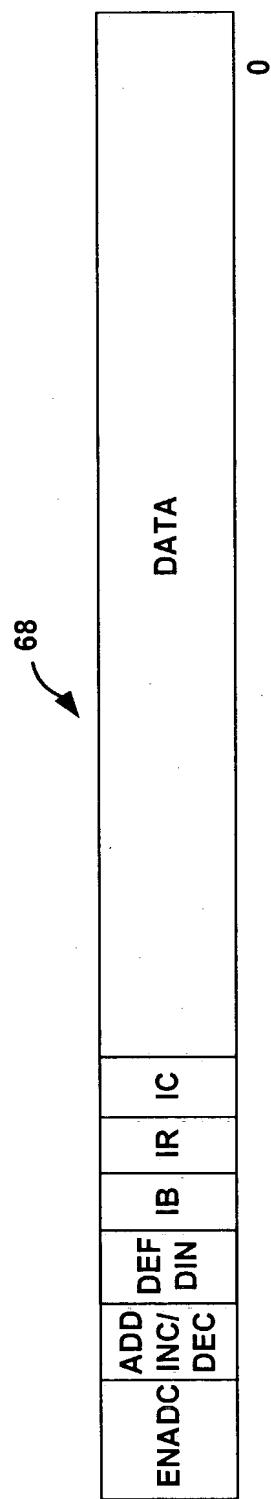
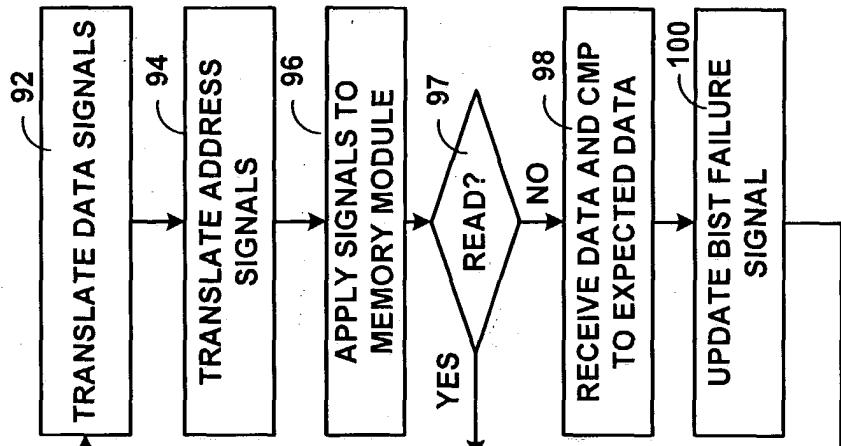
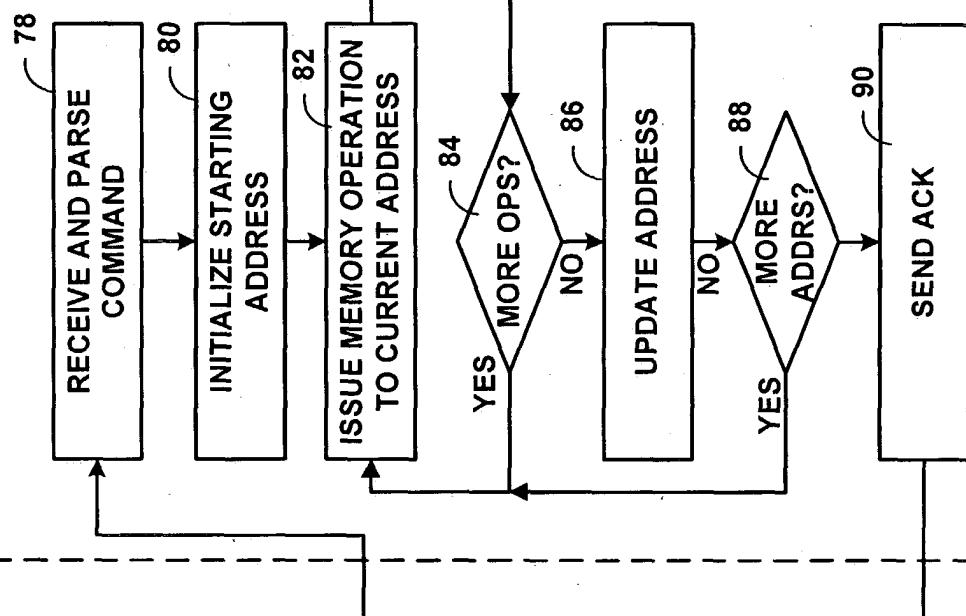


FIG. 9E

MEMORY INTERFACES



SEQUENCERS



SELF-TEST CONTROLLER

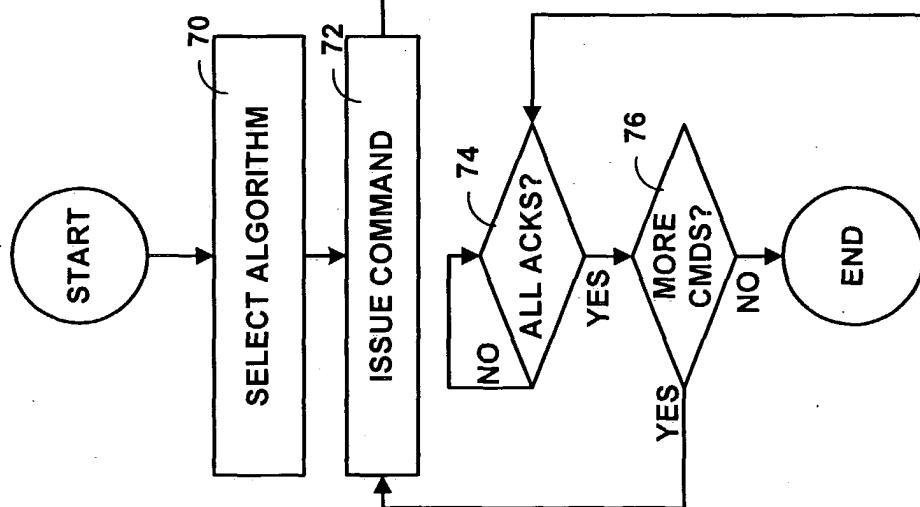


FIG. 10